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    ASIC, 2003. Proceedings. 5th International Conference on
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☐ 2. **Automatic insertion of gated clocks at register transfer level**
    Raghavan, N.; Akella, V.; Bakshi, S.;
    VLSI Design, 1999. Proceedings. Twelfth International Conference On
    7-10 Jan. 1999 Page(s):48 - 54
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☐ 3. **Individual flip-flops with gated clocks for low power datapaths**
    Lang, T.; Musoll, E.; Cortadella, J.;
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☐ 4. **Clock-gating and its application to low power design of sequential circuits**
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☐ 5. **Clock-gating and its application to low power design of sequential circuits**
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